

An Indian-Australian research partnership

Project Title: **Wireline Integrated High-Speed Transceivers with Increased Robustness to Electromagnetic Interference**

Project Number **IMURA0693**

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Research Clusters:

Research Themes:

Highlight which of the Academy's CLUSTERS this project will address? (Please nominate JUST <u>one</u> . For more information, see www.iitbmonash.org)		Highlight which of the Academy's Theme(s) this project will address? (Feel free to nominate more than one. For more information, see www.iitbmonash.org)	
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The research problem

Wireline high-speed transceivers relying on differential signalling form the backbone of chip-to-chip communication systems. The amount of data that needs to be transported from one system to another increases exponentially as novel applications hit the market: as an example, present image sensors of state-of-the-art digital cameras and smart phones are able to detect an image with a resolution exceeding 20 Mpixels, with 12 bit color depth, and at 30-frames/s [1]. To satisfy this requirement, the multi-channel transceivers conveying this data from the camera to the DSP (digital signal processor) must be able to handle a data rate in excess of 10 Gbps.

High-speed wireline communication standards use differential signalling to make these more resistant to common-mode electromagnetic interference (EMI) and crosstalk from neighbouring channels and tracks. The transmission line acts as an undesirable receiving antenna that picks up EMI. For this reason, each wire of a differential transmission line is paired together in a way that an external EMI interference affects both wires simultaneously; thus, creating a common-mode disturbance which varies the transmitter's current drive. In an ideal differential transmitter, a common-mode variation has no effect on the differential signal. In a practical circuit, however, asymmetry and nonlinearities in the transmitter cause common-mode to differential-mode conversion. This is harmful because a common-mode variation caused by injected EMI at the transmission line degrades the differential signal to a point that it becomes unintelligible.

[1] C. Kim, "Circuit Design Techniques for Multimedia Wireline Communications", IEEE ASICON, 2015.

Project aims

This project aims to investigate, design and validate experimentally EMI-resilient wireline transceiver topologies which will outperform the existing transceivers in terms of lower power consumption, an increased data rate and improved resilience to electromagnetic noise.

This design problem is exacerbated by considering that traditional techniques that are employed to design EMI-resilient circuits are not compatible with deep submicron technology nodes: the essential reason for this is the fact that the subsequent reduction in power supply levels weakens the EMI immunity of a circuit, because of the reduced decision levels (digital) and occurrence of hard nonlinearities when an ESD protection is triggered, which happens when the noise signal falls outside the supply rail (analog). The methodology which is proposed in this project will follow the measurement patterns such as described and followed in [2]. In the latter work, the EMI-robustness of an EMI-resilient LVDS transceiver has been characterised by injecting EMI in the differential microstrip PCB traces connected between a LVDS transmitter and LVDS receiver block. An FPGA was programmed to generate a random bit stream in the transmitter, and correlate the received signal to the transmitted one in order to calculate the EMI-induced BER for different EMI levels at different EMI frequencies. In this measurement, the EMI was injected through a TEM cell (transversal electromagnetic cell), which is essentially a miniature benchtop EMC chamber. This methodology is paramount in evaluating the effectiveness of a wireline datalink, especially at a data rate exceeding 1 Gbps, such as targeted in present project.

[2] G. Matig-a, M. R. Yuce, J.-M. Redouté, "An Integrated LVDS Transmitter-Receiver System with Increased Self-Immunity to EMI in 0.18um CMOS", IEEE Transactions on Electromagnetic Compatibility, vol. 58, no. 1, pp. 231-240, Feb. 2016.

Expected outcomes

The main challenge in this task is to increase the transmission speed of wireline systems above several Gbps, while maintaining the EMI-resilience which can presently only be achieved at low data rates. This approach requires a drastic paradigm change as it revolves around two design criteria which are apparently not compatible with each other. This challenge will be mitigated by initially considering low amplitude EMI: the latter simplifies the modelling as a linearized analysis can be followed.

How will the project address the Goals of the above Themes?

This research is focused on the effects of EMI on differential high-speed wireline communication transceiver systems. It is an important research area since wireline communication systems are one of the most prone to failures when subjected to worst case EMI conditions. This project is primarily aimed to find EMI solutions that are integrated using a standard CMOS process. An integrated EMI solution eliminates or minimizes the need for conventional external EMI suppression and mitigation schemes. Having a self-robust differential wireline transmitter and receiver front-end circuit eliminates one of the biggest bottlenecks in the miniaturization and multifunctionalization of electronic systems. It will open the door for the development of differential wireline communication standards that utilize a lower supply voltage, hence decreasing power consumption, increasing speed, and decreasing area footprint. The strategies developed in this project will minimize the research and development effort of such integrated transceivers.

Capabilities and Degrees Required

Candidates should have a MEng or BEng, and have taken CMOS and VLSI design courses. Experience with EDA design tools such as Cadence is a definite bonus. Candidates should be assertive, problem solvers, passionate about analogue and mixed-signal IC design and willing to work independently.

Potential Collaborators

Prof. Shojaei Baghini and Dr. Redoute have been joint supervising and working together since 2011. They are not looking for additional collaborators for this project at this stage.

Select up to **(4)** keywords from the Academy's approved keyword list (**available at www.iitbmonash.org**) relating to this project to make it easier for the students to apply.

Wireline integrated transceivers, CMOS integrated circuits.